Chip Prototypes & Feasibility Studies

Danish Chips Competence Centre

1- Requirements
2- Top-level architecture
3- Block partitioning
4- RTL design
5- Behavioral modeling
6- Functional verification
7- Simulation
8- Design for test insertion
9- Gate-level simulation
10- Formal equivalence checking
11- Partitioning
12- Floor planning
13- Power planning
14- Placement
15- Clock tree synthesis
16- Routing
17- Timing closure
18- Wafer preparation
19- Oxidation and deposition
20- Photolithography and doping
21- Chemical mechanical polishing
22- Backend process steps
23- Die classification
24- Die dicing and die attach
25- Wire bonding
26- Encapsulation
27- Functional testing
28- Parametric testing
29- Burn-in testing
30- Reliability testing
31- Yield classification
32- Final characterization

Steps of a Chip Prototype:

Start

1. System Specification & Architecture Design

2. Functional Design & Circuit Design

3. Physical Design & Physical Verification

4. Fabrication & Packaging

5. Testing & Chip Finishing

Finish

A Feasibility Study at DkCCC Can Provide Detailed Proposals for:

A. High-level Design
Outlines the overall system architecture, key components, and design approach. This includes defining functional requirements, identifying critical interfaces, and establishing a conceptual framework to guide detailed design and implementation.

B. Design Time and Resources
Provides an estimate of the total time required to complete the design phase, along with a breakdown of the human resources, expertise, and tools needed. This ensures efficient allocation of personnel and helps plan project timelines realistically.

C. Cost and Delivery Time
Presents a comprehensive analysis of project costs (including materials, labor, and overhead) alongside a projected delivery schedule. This helps stakeholders evaluate the project's financial feasibility and align expectations with budgetary constraints and deadlines.
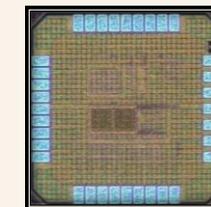
Examples of Prototype Costs at ICELab:

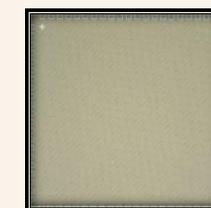**10 packaged 12-pin 1.7mm² High-Precision OpAmp in 180nm**
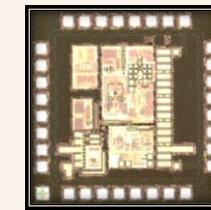
Vendor: Europractice
Foundry: TSMC
Type: mini@sic
Design Phase: 48 weeks
Tapeout Delivery: 12 weeks
Test Phase: 4 weeks
Tapeout Cost: 1,800 EUR
Package Cost: 1,500 EUR

10 packaged 36-pin 1mm² CMOS Temperature Sensor in 65nm

Vendor: Europractice
Foundry: TSMC
Type: mini@sic
Design Phase: 12 weeks
Tapeout Delivery: 16 weeks
Test Phase: 2 weeks
Tapeout Cost: 3,662 EUR
Package Cost: 2,195 EUR

10 packaged 84-pin 3mm² 16-Core SNN in 28nm

Vendor: Europractice
Foundry: TSMC
Type: mini@sic
Design Phase: 48 weeks
Tapeout Delivery: 16 weeks
Test Phase: 12 weeks
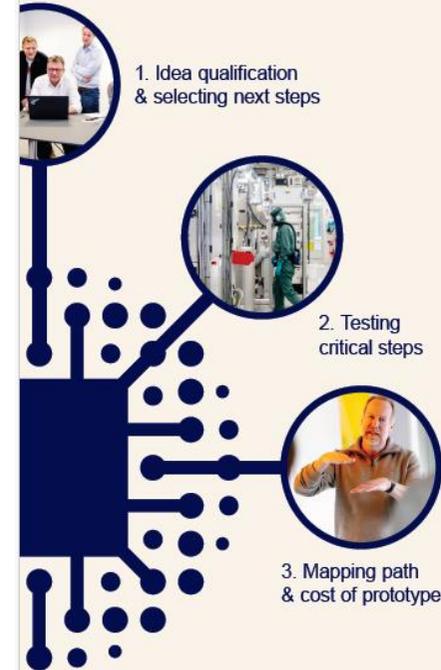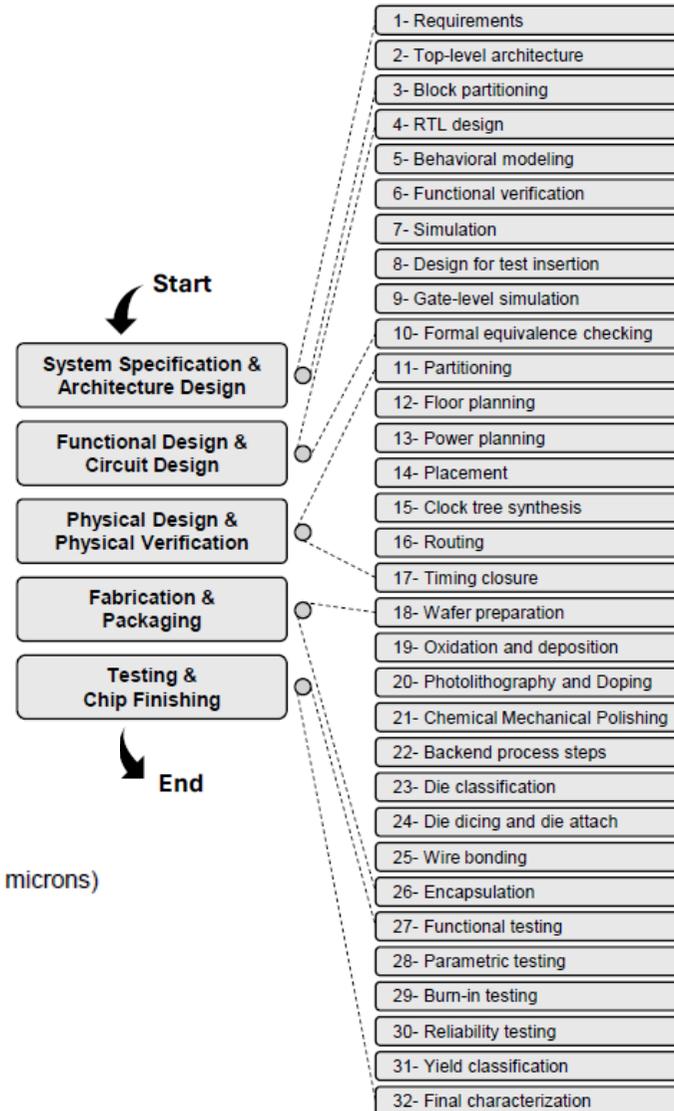Tapeout Cost: 25,200 EUR
Package Cost: 5,000 EUR

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A Feasibility Study can provide detailed proposals for

a) High-level design

b)= Design time & resources

c) Cost and delivery time for samples

10 packaged 36-pin 5mm² chips in 180nm CMOS
- Vendor: Muse
- Foundry: TSMC
- Type: MPW
- Tapeout Cost: 5×(1,250/1mm²) = **6,250 EUR**
- Package Cost: **2,195 EUR** (pad pitch of min. 90 microns)itch of min. 90 microns)
- Tapeout Delivery: 10 weeks

Start

- System Specification & Architecture Design
- Functional Design & Circuit Design
- Physical Design & Physical Verification
- Fabrication & Packaging
- Testing & Chip Finishing

End

1- Requirements
2- Top-level architecture
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1. Idea qualification & selecting next steps

2. Testing critical steps

3. Mapping path & cost of prototype

More Info on: